Session 4 Overview

RF Building Blocks

Chair: *Nikolaus Klemmer, Ericsson Mobile Platforms, Research Triangle Park, NC*

Associate Chair: *Satoshi Tanaka, Hitachi, Tokyo, Japan*

Over the past decade, wireless-enabled devices have evolved from single-purpose, single-band, and single-modulation novelties to highly powerful, ubiquitously available, and ever more lifestyle changing information exchange devices with multi-band and multi-standard modulation capabilities. Growing popularity and per-user capacity requirements from mobile voice and data traffic, multi-purpose wireless information managers and entertainment devices, make RF link capacity the driver for wireless technology development. To deliver on the wireless promise, regulatory bodies and network operators continue to open new frequency bands to accommodate more bandwidth and make use of higher-order modulation formats. These introduce new challenges in the design of RF transceivers.

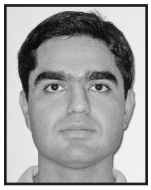
For mobile transmitters, design challenges arise from the need for high-linearity power amplifiers while simultaneously maintaining high power efficiency and low complexity. In addition, interference environments for receivers are becoming more hostile. With a wider range of interfering bands and modulation formats, front-end linearity enhancement and circuit impairment cancellation methods are becoming more crucial. The higher number and wider spread of allocated frequency bands globally pose stringent requirements on the frequency tuning range and noise performance of on-chip oscillators.

The focus of this session is on building blocks for RF transceivers that provide novel contributions to the design of linear, high-efficiency transmitters, receiver front-ends that are able to cope with the presence of strong blockers and modulated interferers, as well as low-noise and high-tuning-range oscillators. Most notably, increased use of digital signal processing and calibration techniques in traditionally analog-only circuit blocks helps to achieve the presented performance increases.

The first three papers of this session describe transmitter building blocks. Paper 4.1 from Stanford shows an implementation of a digital-to-RF converter for use as an OFDM PA. Oversampling and interpolation of the digital amplitude information at RF helps to cope with aliasing artifacts. Paper 4.2 from U Catania and STMicroelectronics describes a 3W CMOS PA with a novel implementation of a closed-loop output load mismatch protection and Paper 4.3 from Arizona State U demonstrates increased power efficiency for polar-modulation PAs via the use of a combination switched-mode and linear power supply regulator system.

Paper 4.4 from Broadcom describes the use of a translational loop around a receiver LNA to cancel blocker signals at the input to the down-conversion mixer, while Paper 4.5 from U Erlangen-Nuremberg and Infineon demonstrates a continuously-on digital LMS-based background calibration scheme for cancellation of down-converter second-order nonlinearity effects. Paper 4.6 from Alfaplus Semiconductor and National Taiwan U makes use of scalable time-to-digital conversion techniques to reduce the SNR requirement, chip area, and power consumption of GFSK demodulators for Bluetooth receivers.

The last two papers focus on low-noise and high-tuning-range oscillators. Paper 4.7 from Epoch Microelectronics and Renesas Technology shows a current re-use technique that allows for low bias-current noise without adding extra bias-generator supply current. Finally, Paper 4.8 from U Pavia and STMicroelectronics shows the beneficial use of tunable current ratios in the windings of a transformer-capacitor resonator to increase oscillator tuning range to over an octave.



4.1 A Digitally Modulated Polar CMOS PA with 20MHz Signal BW **1:30 PM**

A. Kavousian, Stanford University, Stanford, CA

A polar PA employs an array of 64 constant-envelope amplifiers that are activated digitally using 4× oversampling and interpolation to support 64QAM OFDM signals. Implemented in 0.18µm CMOS, the amplifier operates at 1.6GHz with 20MHz signal BW and achieves 7.2% PAE with -26.8dB EVM while delivering 13.6dBm linear output power.

4.2 A 3W 55% PAE CMOS PA with Closed-Loop 20:1 VSWR Protection **2:00 PM**

F. Carrara, Università di Catania, Catania, Italy

A 0.25µm 2V CMOS PA for GSM applications delivers 3W output power with 55% PAE. A closed-loop mismatch protection method is implemented that enables the PA to sustain a 20:1 load VSWR at full power. The circuit enables faster protection lock-in by reducing the number of low-frequency poles in the loop response.

4.3 Combined Linear and Δ-Modulated Switched-Mode PA Supply Modulator for Polar Transmitters **2:30 PM**

J. Kitchen, Arizona State University, Tempe, AZ

A combined linear and Δ-modulated switched-mode PA supply modulator for polar transmitters is designed in a 0.25µm CMOS process. The modulator follows the input envelope and achieves 20dB output DR, a maximum efficiency of 75.5%, and 75dB SNDR for envelope signals up to 4MHz occupied RF BW. For a 1625kb/s 8PSK RF input at 900MHz, polar modulation of a GSM-900 PA provides 10dB ACPR improvement.

4.4 A Blocker Filtering Technique for Wireless Receivers **3:15 PM**

H. Darabi, Broadcom, Irvine, CA

A filtering technique to remove out-of-band blockers in wireless receivers is presented. The circuit employs a feedforward filtering path to produce an arbitrarily narrow frequency response in the LNA, relaxing mixer linearity requirements. A prototype amplifier is implemented in a 65nm CMOS process. A stop-band rejection of over 21dB is achieved.

4.5 A 0.13µm 1.5V CMOS I/Q Downconverter with Digital Adaptive IIP2 Calibration **3:45 PM**

K. Dufrene, University of Erlangen-Nuremberg, Erlangen, Germany

A low-voltage I/Q downconverter with digital adaptive IIP2 calibration is presented. The system maintains high linearity over time by continuously updating tuning codes in response to varying operating conditions. A prototype is fabricated in a 0.13µm RF CMOS process. At 2GHz LO, it draws 48mA from a 1.5V supply.

4.6 A Delay-Line-Based GFSK Demodulator for Low-IF Receivers **4:15 PM**

H-S. Kao, Alfaplus Semiconductor, Hsin-Chu, Taiwan

A low-power GFSK demodulator employing a self-calibrated delay line and DSP circuits achieves an SNR of 14.9dB. Without any accurate analog circuits and oversampling clocks, the demodulator performs detection for frequency offsets up to ±350kHz. Fabricated in a 0.18µm CMOS process, it occupies 0.26mm^2 and consumes 2mA from a 1.8V supply.

4.7 A 4.5GHz LC-VCO with Self-Regulating Technique **4:45 PM**

A. Dec, Epoch Microelectronics, Hawthorne, NY

A 1.8mA, -116dBc/Hz phase noise at 1MHz offset, 4.1-to-5.1GHz LC-VCO is implemented in 0.18µm SOI BiCMOS process. A low supply pushing of 800kHz/V is achieved with the proposed self-regulating technique without using any large internal or external capacitors.

4.8 A 3.2-to-7.3GHz Quadrature Oscillator with Magnetic Tuning **5:00 PM**

G. Cusmai, Università di Pavia, Pavia, Italy

A quadrature oscillator employs a transformer-capacitor network as an energy tank. Frequency tuning is done by varying the transformer magnetic field via the ratio of currents in the two windings. Realized prototypes have a 3.2 to 7.3GHz frequency tuning range, a phase noise FOM of 176.5dB at 3.2GHz, 170.5dB at 6.4GHz, and 164dB at 7GHz, all calculated at 10MHz offset, and a phase error of <1.5°.